

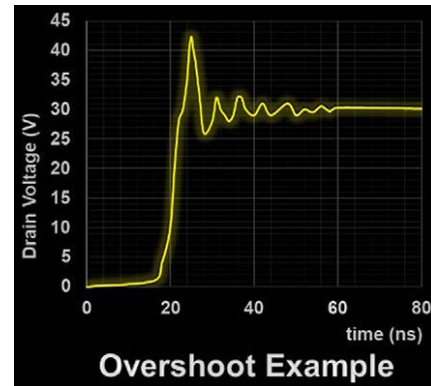


# The 45 V Sweet Spot for Higher Efficiency Synchronous Rectification: 45 V TrenchFET<sup>®</sup> Gen IV MOSFETs

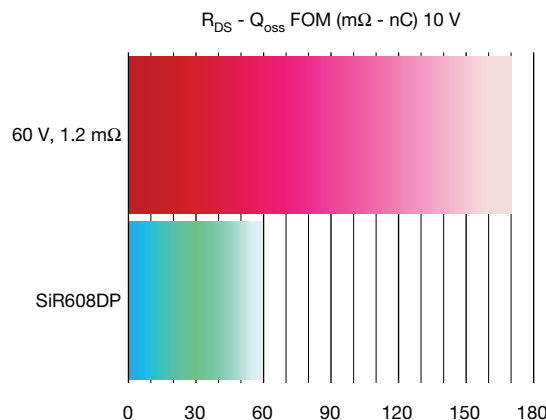
By Brian Terng

- Achieve higher efficiency overall and increase peak efficiency
- Typical  $R_{DS(on)}$  is 1 m $\Omega$  in 6 mm by 5 mm footprint
- Low  $Q_g$  and  $Q_{oss}$  for switching
- Reduce power loss during channel, diode conduction, and switching
- 12.5 % more safety margin than identical 40 V rated solutions
- 65 % lower  $R_{DS} - Q_{oss}$  FOM than 60 V devices

Designers of power conversion circuitry are often forced by certain transient conditions to specify a 60 V power MOSFET in synchronous rectification applications where a 40 V MOSFET would deliver significantly better efficiency. An undesired transient spike usually occurs at the MOSFET's drain node, with a magnitude exceeding either the derating boundary or 40 V for several ns to ms. If the overshoot is less than 45 V, a family of 45 V MOSFETs from Vishay Intertechnology provides the extra margin of headroom to mitigate the voltage transients, while delivering significantly better FOM than any 60 V MOSFET on the market.



Vishay' 45 V TrenchFET<sup>®</sup> Gen IV products reach a sweet spot between performance FOMs and safety margin. Their 45 V breakdown voltage means a 12.5 % greater safety margin than 40 V rated MOSFETs with similar on-resistance characteristics. The typical  $R_{DS(on)}$  is as low as 1 m $\Omega$  in the 6 mm by 5 mm footprint and reduces power loss during channel conduction, while their  $R_{DS(on)} - Q_{oss}$  FOM is 65 % lower than the lowest  $R_{DS(on)}$  60 V device used in these applications (Fig. 1).



**Fig. 1 - Comparison of  $R_{DS(on)} - Q_{oss}$  FOM of Vishay Siliconix' Flagship 45 V TrenchFET Gen IV Device, the SiR608DP, and a 60 V Device With the Same 1.2 m $\Omega$  Maximum On-Resistance**

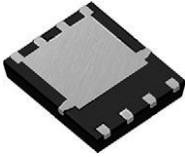
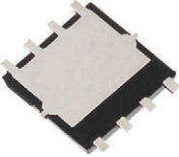
## The 45 V Sweet Spot for Higher Efficiency Synchronous Rectification: 45 V TrenchFET® Gen IV MOSFETs

The improved output charge,  $Q_{oss}$ , potentially reduces the power loss from charging and discharging the output capacitance during switching. The power savings are realized across the entire load range from 0 A to 100 % of output. This improvement combination provides energy savings and offers a reliable solution to increase peak efficiency and achieve higher efficiency overall.

### MEASURING THE SiR608D'S EFFICIENCY

45 V n-channel MOSFETs are currently available through multiple manufacturers. The availability of multiple sources in compatible package footprints reduces the risk of a discontinued supply. How do we know that the SiR608DP is more efficient than the competition in practical circuits? Vishay performed tests using an off the shelf DC/DC power supply module, a 1/8 brick, which steps down from 48 V to 3.3 V. This power supply employs a full-bridge isolated topology with a typical switching frequency of 140 kHz. The module has an interleaved PCB winding transformer. Tuning components other than the MOSFET devices was unfeasible, as the schematic of the design is unavailable to Vishay.

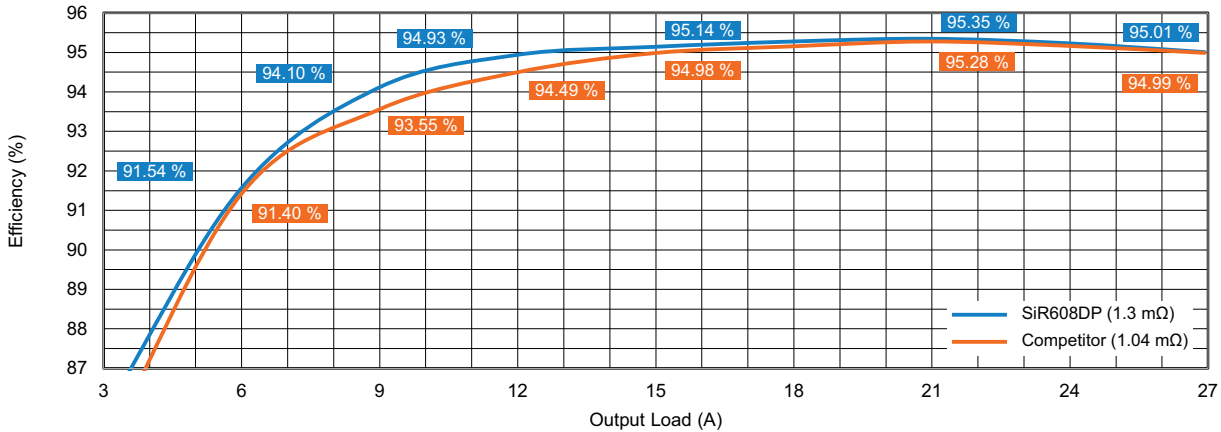
We swapped out the provided MOSFETs on the secondary side to benchmark the SiR608DP and the 45 V device from the other vendor. Table 1 shows a comparison of the specifications of the SiR608DP and the competing device.

| TABLE 1 - COMPARISON OF DEVICES USED FOR <a href="#">SiR608DP</a> BENCHMARK TEST |      |  |   |
|--|------|--|---|
| PART NUMBERS   |      | SiR608DP   | COMPETITOR  |
| Package type   |      | PowerPAK® SO-8<br> | 6 x 5 package<br> |
| $V_{DS}$ (V)   |      | 45   | 45  |
| $R_{DS(on)}$ (mΩ) at 10 V  | Typ. | 1  | 0.8   |
|  | Max. | 1.2  | 1   |
| $Q_g$ (nC) at 10 V   |      | 111  | 122   |
| $Q_{gd}$ (nC)  |      | 8  | 22  |
| $Q_{gs}$ (nC)  |      | 26   | 30  |
| $C_{oss}$ (pF)   |      | 1244   | 1860  |

Both devices come in packages with a 6 mm by 5 mm footprint. It is interesting to note that maximum on-resistance of the competing device, which translates into channel conduction losses, is about 15 % lower than the SiR608DP. However, the SiR608DP outshines the competing device when it comes to gate charge ( $Q_g$ ) and output capacitance ( $C_{oss}$ ). To put the improved dynamic characteristics in perspective, the SiR608DP provides 10 % better  $Q_g$  and 33 % better  $C_{oss}$ . The improved  $Q_g$  and  $C_{oss}$  theoretically reduce power losses from gate driving, switching, and during diode conduction, simultaneously.

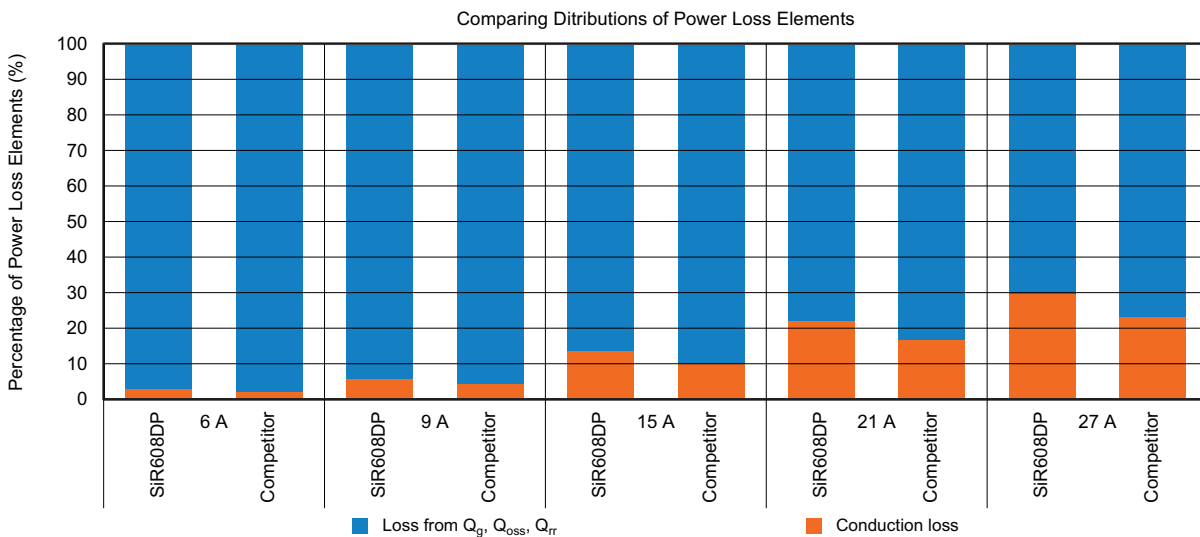
How this translates into efficiency is shown in Fig. 2, where the blue line represents the SiR608DP and the red line the competing device. At every current level, the SiR608DP solution achieves higher efficiency overall and increases peak efficiency. The efficiency measurements were taken at 3 A load steps, starting at the maximum current. At each step the module temperature was allowed to stabilize before the efficiency was recorded.

## The 45 V Sweet Spot for Higher Efficiency Synchronous Rectification: 45 V TrenchFET<sup>®</sup> Gen IV MOSFETs



**Fig. 2 - The SiR608DP and Competing Device Efficiency Comparison, Test Conditions: 48 V Input Voltage, 3.3 V Output Voltage, 1/8 Brick,  $F_{SW} = 140$  kHz**

Vishay’s analysis suggests that the switching elements are the dominant loss contributors in this module, while conduction-related losses are estimated to be around 30 % of the total power loss. The gap between the efficiencies of the two devices peaks at 0.44 % at the 12 A load point. The chart in Fig. 3 compares the loss contributions for both parts at the measurement points.



**Fig. 3 - Power Loss Distribution for the SiR608DP and Competing Device by DC and Dynamic Elements Across the Current Loads**

## The 45 V Sweet Spot for Higher Efficiency Synchronous Rectification: 45 V TrenchFET<sup>®</sup> Gen IV MOSFETs

The conduction loss rarely exceeded 30 % of the total power loss in the testing, as both devices have very low typical  $R_{DS(on)}$ . The blue partition, which represents the power loss from  $Q_g$ ,  $Q_{oss}$ , and  $Q_{rr}$ , reveals a much higher contribution to the majority of the power loss. Switching at 140 kHz, the lower  $Q_g$  and  $Q_{oss}$  of the SiR608DP helped the circuitry cut the wasted power from switching by 25 % compared to designs using the competitor's product.

Although the  $R_{DS(on)}$  of the competitor's device was marginally lower, the conduction loss difference was not enough to compensate for the power loss generated by the switching parameters, such as  $Q_g$  and  $Q_{oss}$ , even at the full load of the power supply tested. When a design requires paralleling more parts in applications in which the supply power exceeds the kW level, the advantage of marginally lower on-resistance gradually disappears, while losses unrelated to  $R_{DS(on)}$  could become more pronounced due to their cumulative nature.

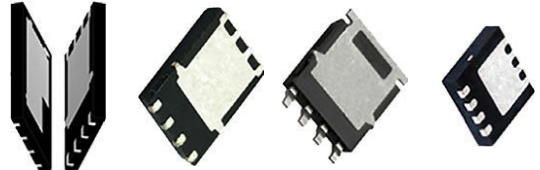


**Fig. 4 - Power Loss Distribution for the SiR608DP and Competing Device at Output Load of 27 A**

## The 45 V Sweet Spot for Higher Efficiency Synchronous Rectification: 45 V TrenchFET® Gen IV MOSFETs

### WIDE ARRAY OF PACKAGE OPTIONS

The Vishay Siliconix 45 V portfolio currently offers a choice of several different package types (Table 2) to meet various design configurations. This portfolio targets a diverse range of applications in battery management, computing, industrial, motor drive control, power supplies, power tools, servers, and telecommunication equipment.

| TABLE 2 - $V_{DS} = 45\text{ V}$ , $V_{GS} = +20\text{ V} / -16\text{ V}$ POWER MOSFET PORTFOLIO |                 |  |       |               |       |                  |                  |                   |                           |                          |                          |                          |
|--|-----------------|--|-------|---------------|-------|------------------|------------------|-------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| $V_{DS}$<br>(V)  | $V_{GS}$<br>(V) | Max. $R_{DS(ON)}$<br>( $m\Omega$ )   |       | $Q_g$<br>(nC) |       | $Q_{gs}$<br>(nC) | $Q_{gd}$<br>(nC) | $C_{OSS}$<br>(pF) | (6 x 5) mm <sup>2</sup>   |                          |                          | (3 x 3) mm <sup>2</sup>  |
|  |                 | 10 V   | 4.5 V | 10 V          | 4.5 V |                  |                  |                   | PowerPAK®<br>SO-8DC       | PowerPAK®<br>SO-8        | PowerPAK®<br>SO-8L       | PowerPAK®<br>1212-8S     |
|  |                 |  |       |               |       |                  |                  |                   |                           |                          |                          |                          |
| 45   | +20 / -16       | 1.2  | 1.8   | 111           | 50.5  | 26               | 7.8              | 1244              | <a href="#">SiDR608DP</a> | <a href="#">SiR608DP</a> | -                        | -                        |
|  |                 | 2.71   | 3.97  | 46.7          | 21.4  | 11.1             | 3.6              | 630               | -                         | <a href="#">SiR150DP</a> | -                        | -                        |
|  |                 | 2.83   | 4.1   | 46.7          | 21.4  | 11.1             | 3.6              | 630               | -                         | -                        | <a href="#">SiJ150DP</a> | <a href="#">SiSS50DN</a> |

Devices in the PowerPAK SO-8 (SiR608DP, SiR150DP) and PowerPAK 1212-8S (SiSS50DN) provide conventional surface-mount solutions. The PowerPAK packages contribute negligible additional resistance and maximize the performance of the silicon. The compact size of the PowerPAK 1212-8S is particularly useful for PCBs with limited real estate.

In the PowerPAK SO-8L, the SiJ150DP is optimized for wave soldering. The protruding leads allow for visual inspection. The flexible gull-wing leads increase resilience to mechanical stress and board flexing.

In the PowerPAK SO-8DC, the SiDR608DP supplies a double-cooled feature to facilitate heatsinking and to enable higher power density. The connection between the package and heatsink requires the application of a thermal interface material for the most effective thermal transfer. The exposed pad on top of the package is an active source connection. Selected designs in which unplanned coupling and EMI are issues should choose interface materials with electrical isolation properties.

### CONCLUSION

Vishay's 45 V TrenchFET Gen IV portfolio offers high performance in a variety of packaging options. The products help designers increase efficiency and power density in a broad range of applications, including battery switch, motor drive control, and synchronous rectification in AC/DC and DC/DC power supplies. All the products mentioned have been released for mass production. Please visit Vishay's website for datasheets and collateral to support your design activities.

### AUTHOR

Brian Teng is currently part of the market development team in Vishay Intertechnology's MOSFET division.